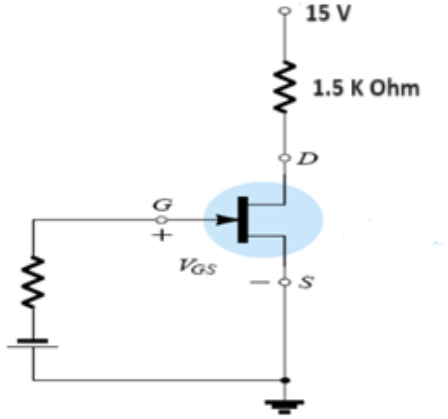
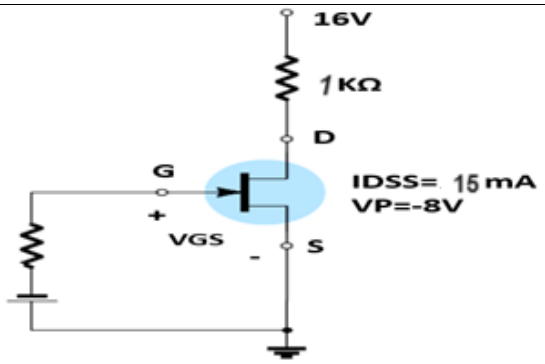
PART 1
FET Transistor

Q1. For the fixed-bias JFET shown below if V_{DS} =7.5V, what is the value of I_D?



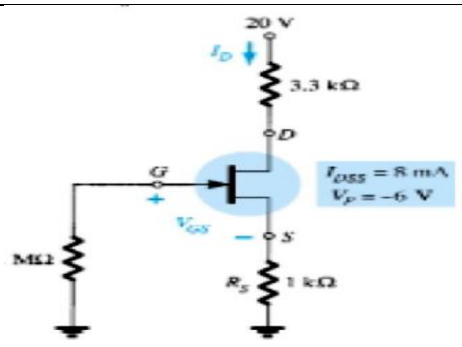
5.5 mA	A
2 mA	B
5 mA	C
2.5 mA	D

Q2. For the given circuit in figure below, if I_D=8mA what is the value of V_{DS}?



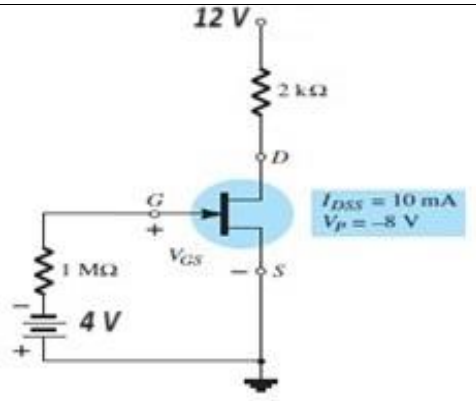
10 V	A
6 V	B
8 V	C
4 V	D

Q3. For self-bias configuration circuit, if I_D=3mA, then V_{DS} is……..

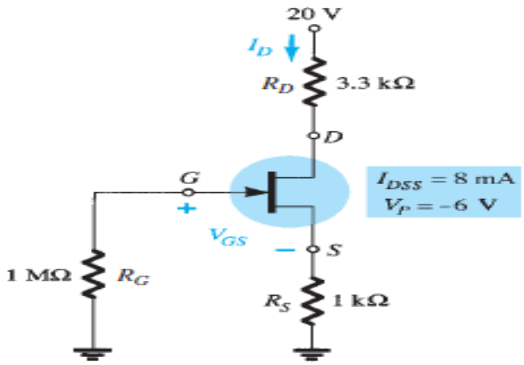


17 V	A
7.1 V	B
1.7 V	C
1.6 V	D

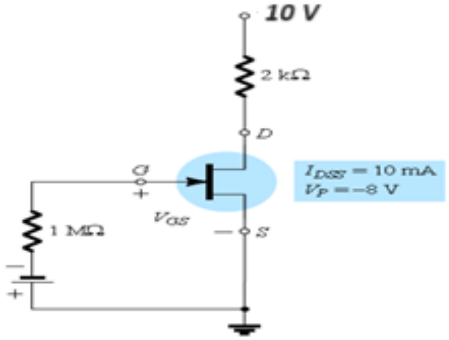
Q4. For the circuit shown below, I_D = …….

	5.5 mA	A
	2 mA	B
	2.5 mA	C
	3.5 mA	D

Q5. For the circuit shown below, if V_{GS} = -3V, then I_D =……

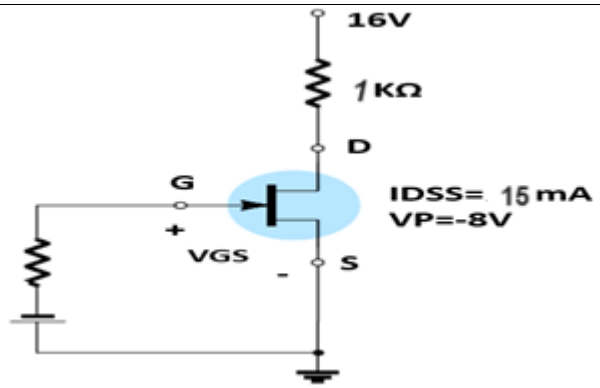
	8 mA	A
	2 mA	B
	4 mA	C
	Zero	D

Q6. For the circuit shown in figure below, if I_D = 2.5 mA, then V_{DS} is…….

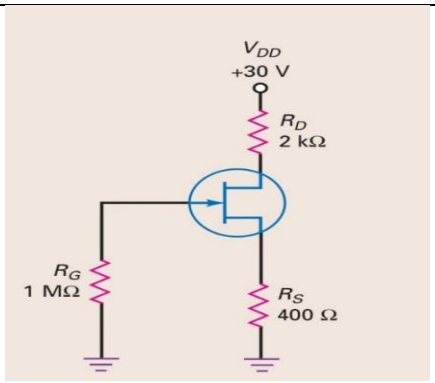
	3 V	A
	5 V	B
	4 V	C
	0V	D

Q7. For the given circuit in figure below, if V_{DS}=6V what is the value of I_D?

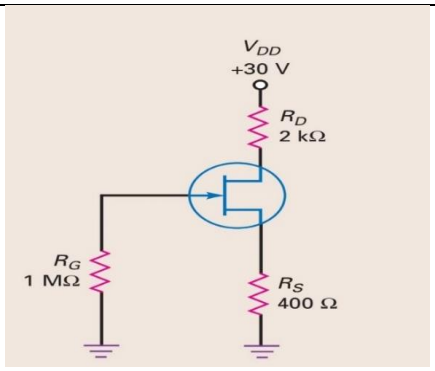
	10 mA	A

	5 mA	B
	4 mA	C
	16 mA	D

Q8. For the circuit given below, if I_D = 10 mA what is the value of V_{DS}?

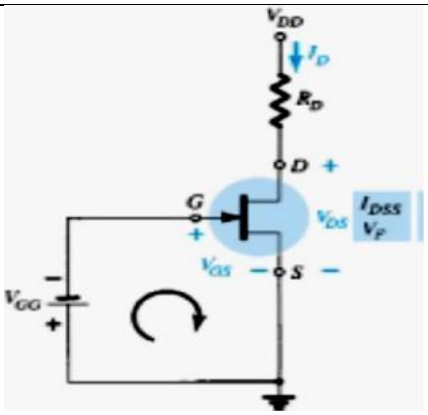
	9 V	A
	8 V	B
	6 V	C
	1 V	D

Q9. For the circuit given below, if I_D = 10 mA what is the value of V_{GS}?

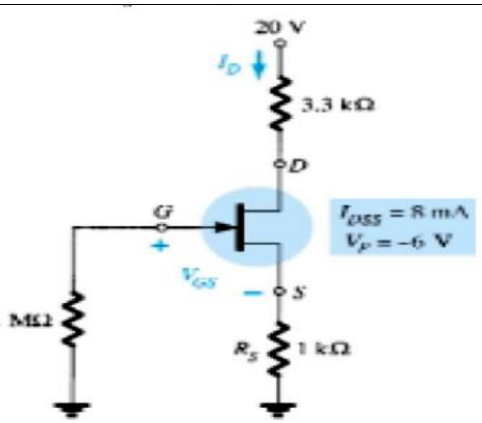
	Zero	A
	-4 V	B
	4 V	C
	-2 V	D

Q10. For the fixed biased configuration JFET circuit, Vs is ……

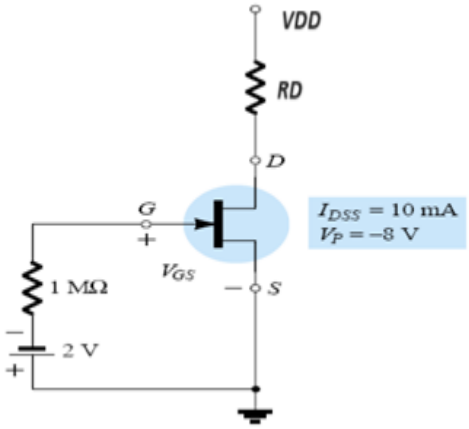
	Zero	A
	0.7 V	B

	-0.7 V	C
	1.4 V	D

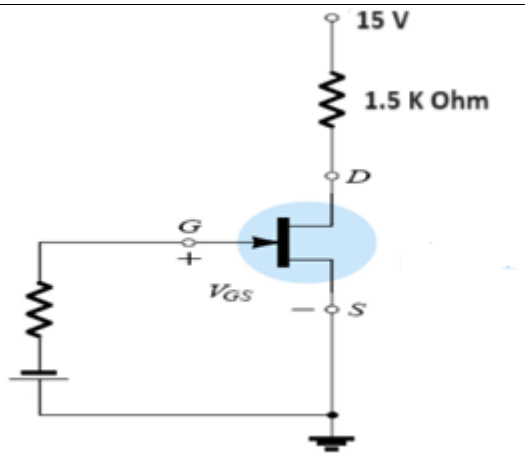
Q11. For self-bias configuration circuit, if I_D=2.6 mA, then Vs is……..

	2.6 V	A
	3 V	B
	1.8 V	C
	1.6 V	D

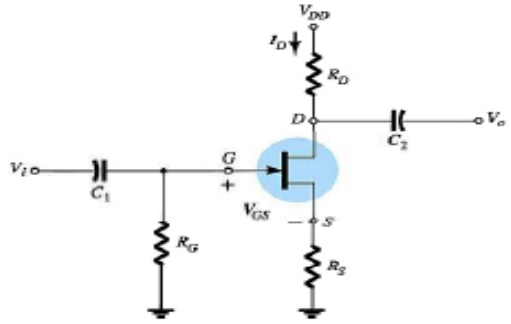
Q12. For the fixed-bias JFET shown below, what is the value of the drain current I_D?

	6.250 mA	A
	2.650 mA	B
	5.625 mA	C
	0.650 mA	D

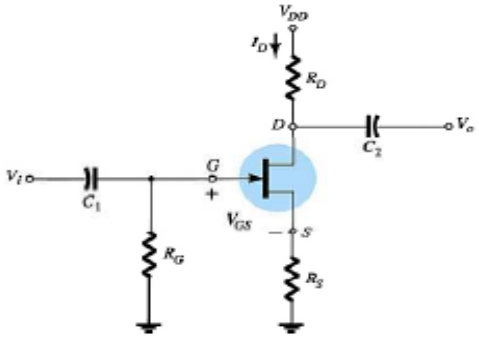
Q13. For the fixed-bias JFET shown below if I_D=10mA, what is the value of the V_{DS}?

	7.5 V	A
	4 V	B
	5.75 V	C
	0 V	D

Q14. In a Self-bias JFET circuit shown below, V_{DS} is determined from the equation .....

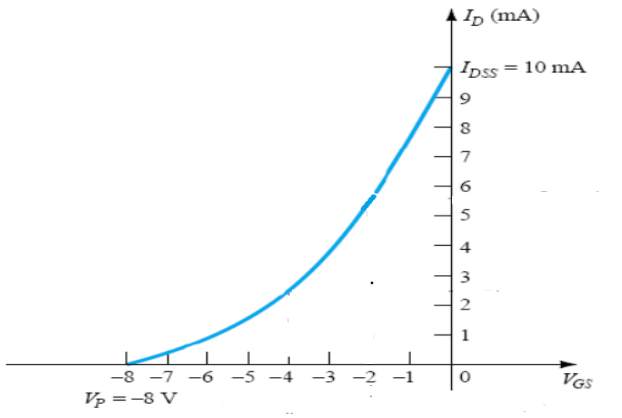
	$V_{DS} = V_{DD} - I_D \cdot R_S$	A
	$V_{DS} = V_{DD} + I_D (R_S + R_G)$	B
	$V_{DS} = V_{DD} - I_D (R_S + R_D)$	C
	$V_{DS} = V_{DD} - I_D \cdot R_D$	D

Q15. For the n-channel JFET shown, if Rs= 500Ω and I_D=6 mA what is the value of V_{GS}?

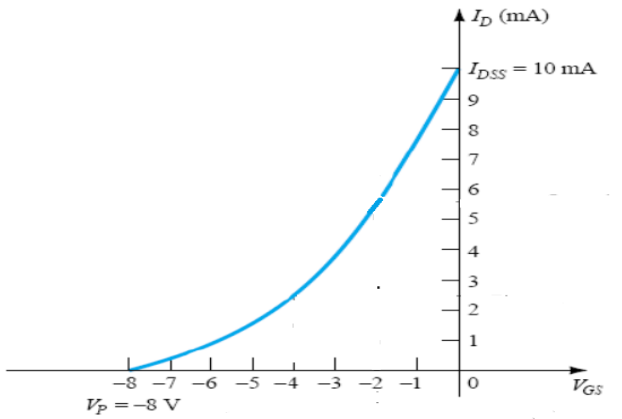
	-6 V	A
	3 V	B
	-3 V	C
	Zero	D

Q16. For JFET's characteristics shown, if I_D = 5.6mA, what is the value of V_{GS}?

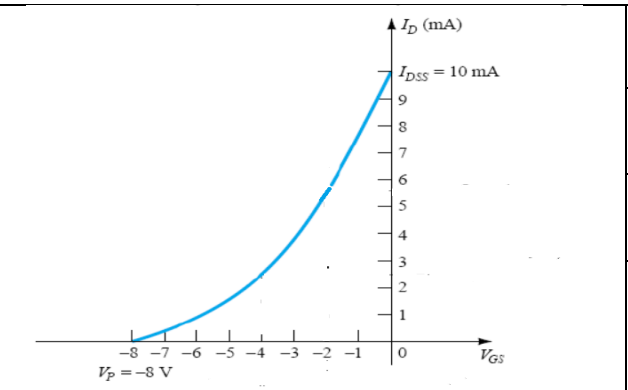
	-1 V	A
	-3 V	B

	Zero	C
	-2 V	D

Q17. For the FET transfer characteristics, when $I_D=I_{DSS}/2$, then V_{GS} is ……

	Zero	A
	-3V	B
	-2.4 V	C
	-6V	D

Q18. For the FET transfer characteristics, when $V_{GS}=V_p/2$, then I_D = ……

	Zero	A
	2.5 mA	B
	5 A	C
	10 A	D

Q19. What is the value of drain current when V_{GS} = pinch-off voltage V_p?

Zero	A

> I_{DSS}	B
< I_{DSS}	C
= I_{DSS}	D
Q20. For an n-channel FET, What is the direction of current flow?	
Source to drain	A
Drain to source	B
Gate to source	C
Gate to drain	D
Q21. What is the value of I_D when V_{GS} is less than the pinch-off voltage V_p?	
Zero	A
> I_{DSS}	B
Maximum	C
< I_{DSS}	D
Q22. Which of the following statement is true about FET?	
It has high output impedance	A
It has high input impedance	B
It has low input impedance	C
It does not offer any impedance	D
Q23. When will maximum drain current flows in a FET?	
$V_{GS} = 0$	A

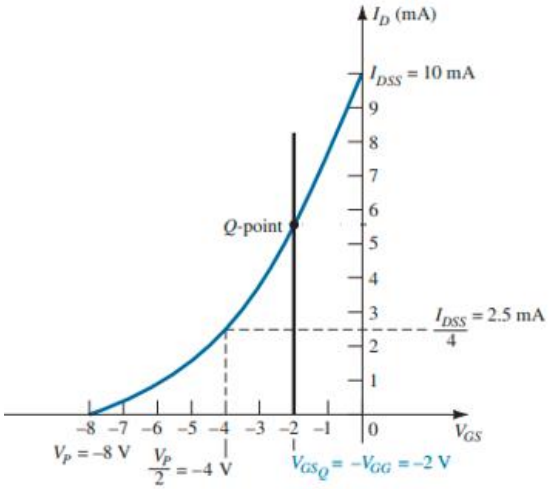
$V_{GS} = V_p$	B
$V_{DS} \leq V_p$	C
$V_{DS} \geq V_p$	D
Q24. In shorthand method, if ($V_{GS} = V_p /2$) then ……	
$I_D = 0$	A
$I_D = I_{DSS}$	B
$I_D = 0.5\ I_{DSS}$	C
$I_D = 0.25\ I_{DSS}$	D
Q25. If V_{GS} = -2 V, then V_{GG}=…….	
2V	A
-4V	B
-5V	C
-2V	D
Q26. The Shockley equation is ……	
$I_D = I_{DSS}[1 - \frac{V_{GS}}{Vp}]^2$	A
$I_D = I_{DSS}[1 - \frac{V_{GS}}{Vp}]^3$	B
$I_D = I_{DSS}[1 - \frac{V_{GG}}{Vp}]^2$	C
$I_D = I_{DSS}[2 - \frac{V_{GS}}{Vp}]^2$	D
Q27. JFET is …….	
Bipolar field junction	A

Transistor field junction	B
Effect transistor field	C
Junction field effect transistor	D
Q28. If $I_{DSS} = 10\ mA$, $V_{GS} = 0V$, then I_D= …….	
5m A	A
7m A	B
10m A	C
13m A	D
Q29. The maximum current in JFETs is defined as I_{DSS} and occurs when V_{GS} = ……	
0 V	A
∞	B
Maximum	C
0.7 V	D
Q30. For the FET transfer characteristics when **I_D=0**, then V_{GS} = …….	
V_p	A
Zero	B
undefined	C
minimum	D
Q31. For the FET transfer characteristics when I_D=I_{DSS}, then V_{GS} is …….	
-1.8 V	A

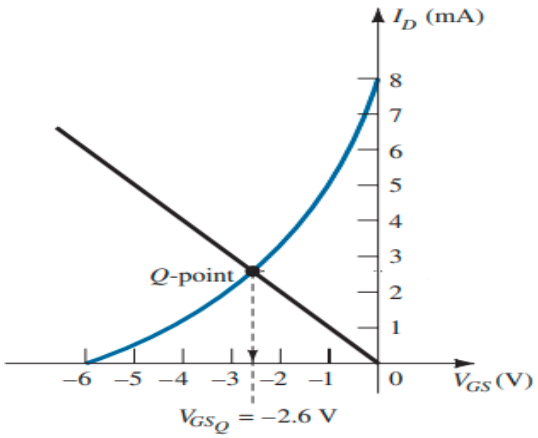
-3V	B
0 V	C
-6V	D
Q32. I_{DSS} is ……	
the drain current with the drain-source open-circuited	A
the drain current at cutoff	B
the maximum possible drain current	C
the zero-drain current	D
Q33. The names of the three terminals of JFET are ……	
cathode, anode, grid	A
emitter, base, collector	B
source, gate, drain	C
none of the above	D
Q34. A JFET is a …… controlled device.	
current	A
voltage	B
both current and voltage	C
none of the above	D
Q35. For a self-bias configuration of n-channel JFET; if $I_D = 10mA$ and $V_{GS}=-5V$, what is the value of source resistance R_S?	
250 Ω	A

500 Ω	B
750 Ω	C
1500 Ω	D
Q36. In a FET, the control variable is:	
V_{GS}	A
V_{DS}	B
V_{GG}	C
I_D	D
Q37. The gate of a JFET is …… biased.	
Reverse	A
Forward	B
Reverse and forward	C
Open circuited	D
Q38. For all FETs ……	
$I_D = I_S$	A
$I_D = 0$ mA	B
$I_D = I_G$	C
$I_S = I_G$	D
Q39. In JFET, using Shockley equation, when $V_{GS} = 0$, then ……	
$I_D = 0$	A

$I_D = I_{DSS}$	B
$I_{DSS} = 0$	C
$V_p = 0$	D
Q40. The gate voltage in a JFET at which drain current becomes zero is called ……. voltage	
Saturation	A
Pinch-off	B
Active	C
Cut-off	D
Q41. The channel of a JFET is between the ……	
gate and drain	A
drain and source	B
gate and source	C
input and gate	D
Q42. What is the value of V_{GS} when $I_D = I_{DSS}$?	
= Zero	A
> pinch-off voltage	B
< pinch-off voltage	C
= pinch-off voltage	D
Q43. For the transfer characteristics of JFET (fixed bias circuit) shown the value of I_{DQ} ?	
5.6 mA	A
6.5 mA	B

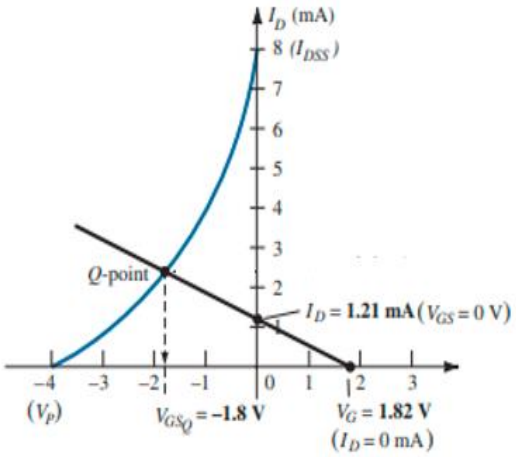
	6 mA	C
	0 mA	D

Q44. For the transfer characteristics of JFET (self bias circuit) shown the value of I_{DQ}?

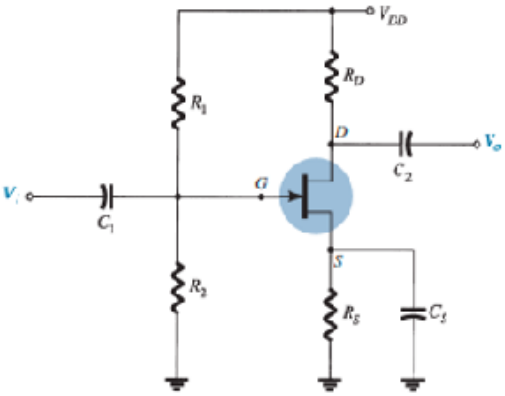
	Zero mA	A
	2 mA	B
	2.6mA	C
	-2.6 mA	D

Q45. For the transfer characteristics of JFET (voltage divider circuit) shown the value of I_{DQ}?

	2.4 mA	A
	1.21 mA	B
	-2 mA	C

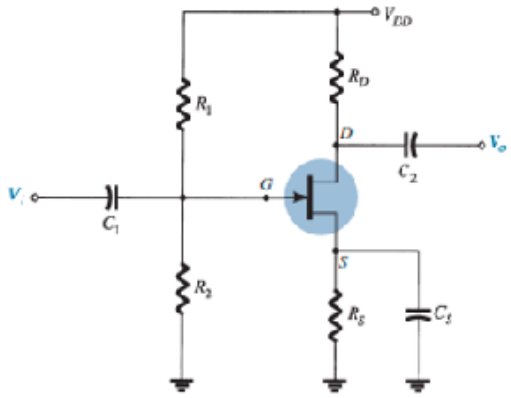
	1.82 mA	D

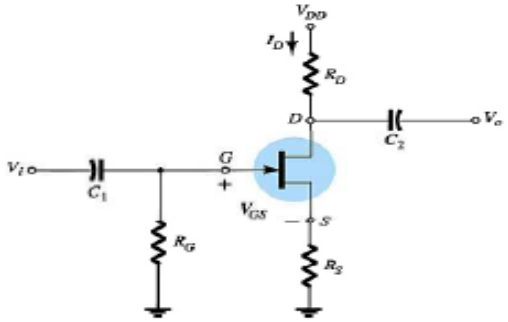
Q46. For the the voltage divider circuit of FET transistor below, V_G= …….

	$V_G = \frac{VDD\ R1}{R1+R2}$	A
	$V_G = \frac{VDD\ R2}{R1+R2}$	B
	$V_G = \frac{VDD}{R1+R2}$	C
	$V_G = \frac{VDD\ RD}{R1+R2}$	D

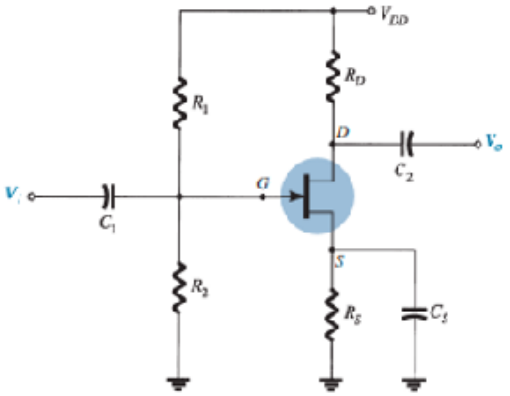
Q47. For the the voltage divider circuit of FET transistor below, V_D= …….

	$V_D = V_{DD} - I_D R_S$	A
	$V_D = V_{DD} - I_D R_D$	B
	$V_D = 0$	C

	$V_D=V_{DD}-V_S$	D

Q48. In a Self-bias JFET circuit shown below, V_{GS} is determined from the equation ……		
	$V_{GS} = V_{DD}$	A
	$V_{GS} = - I_D R_S$	B
	$V_{GS} = R_G - I_D R_S$	C
	$V_{DS} = V_G$	D

Q49. For the the voltage divider circuit of FET transistor V_{GS}= …….



$V_{GS}=V_G-I_D R_S$	A
$V_{GS}=V_G-I_D R_2$	B
$V_{GS}=V_G-I_D R_1$	C
$V_{GS}=V_G-I_D R_D$	D

Q50. JFET transistor is a ……

current-controlled device	A
voltage-controlled device	B
power-controlled device	C
energy-controlled device	D

Q51. The depletion regions are wider toward the drain end of the channel because the reverse-bias voltage between the gate and the drain is ……

greater than that between the gate and the source.	A
less than that between the gate and the source.	B
equals infinity	C
equals zero	D

Q52. The output characteristic curve of a FET transistor is divided into:	
saturation region and ohmic region	A
saturation and closed region	B
ohmic and cutoff region	C
source and gate region	D
Q53. Reverse biasing of the gate-source junction produces a depletion region in the n-channel and thus….	
decreases its resistance	A
make it equal to zero	B
increases its resistance	C
make it equal to infinity	D

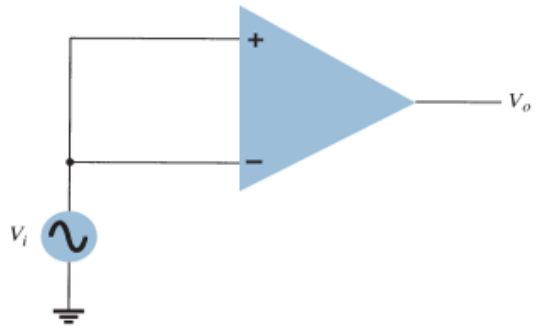
Q54. Input impedance at the gate is very high, thus the gate current ……	
$= \infty$	A
$= I_D$	B
$= I_S$	C
= zero	D
Q55. The channel width can be controlled by varying the gate voltage, and thereby, …… can also be controlled	
I_G	A
I_D	B
I_S	C

I_C	D

Q56. The depletion regions are wider toward the drain end of the channel because :	
reverse-bias between gate and drain > reverse-bias between gate and source	A
reverse-bias between source and drain > reverse-bias between gate and source	B
reverse-bias between gate and drain < reverse-bias between gate and source	C
reverse-bias between source and drain > reverse-bias between gate and drain	D

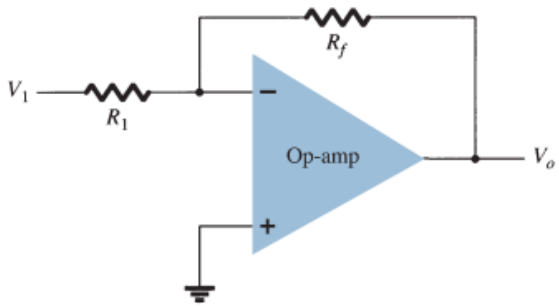
PART 2
Operational Amplifier

Q1:The gain of Operational Amplifier mode shown is……



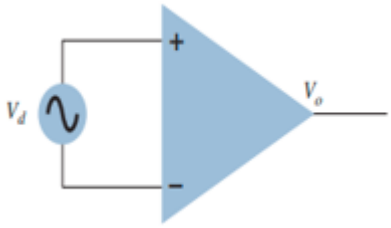
Very low	A
Very high	B
unity	C
zero	D

Q_2. The output voltage of an OP-amp shown is:



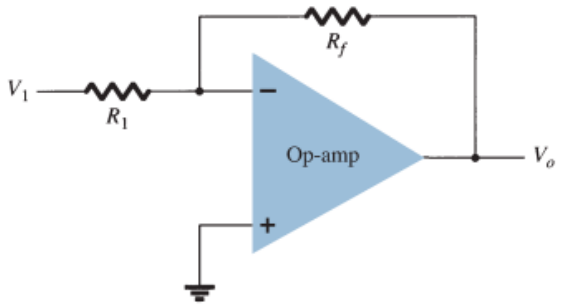
$V_O = -\frac{R_f}{R1}$ vi	A
$V_O = -\frac{R_1}{Rf}$ vi	B
$V_O = \frac{R_f}{R1}$vi	C
$V_O = (1+\frac{R_f}{R1})$ vi	D

Q_3. The gain of Operational Amplifier mode shown is……



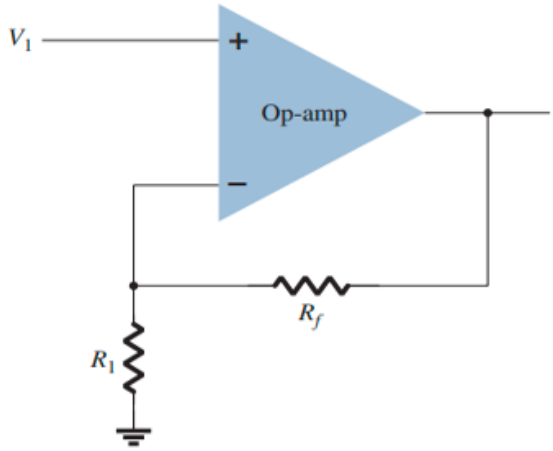
Very low	A
Very high	B
unity	C
zero	D

Q_4. If the circuit of figure shown has R1= 100KΩ and Rf =500 KΩ ,what output voltage results for an input of V1= 2v?



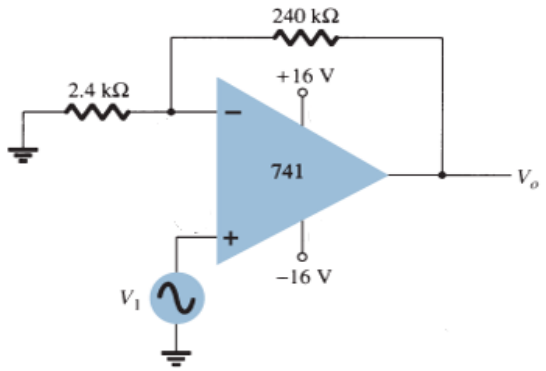
8 v	A
2 v	B
2.5 v	C
-10 v	D

Q5. The operational amplifier circuit shown in the figure works as …….



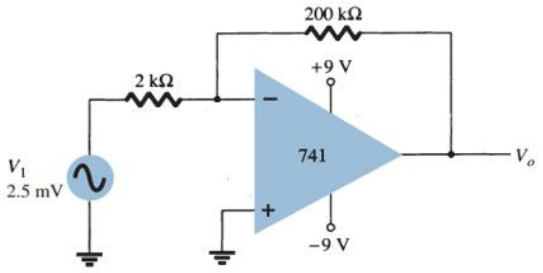
Inverting amplifier	A
Integrator	B
Noninverting Amplifier	C
Differentiator	D

Q6. Calculate the output voltage from the circuit of figure shown for an input of 120 μV.

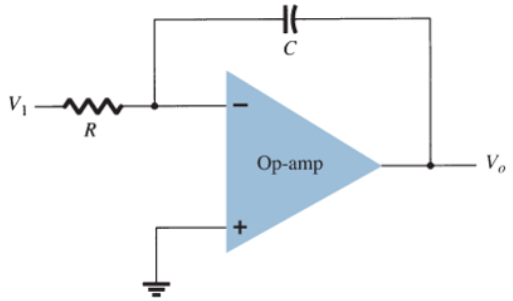


12.12 mV	A
11.12 V	B
4 V	C
-12.12 mV	D

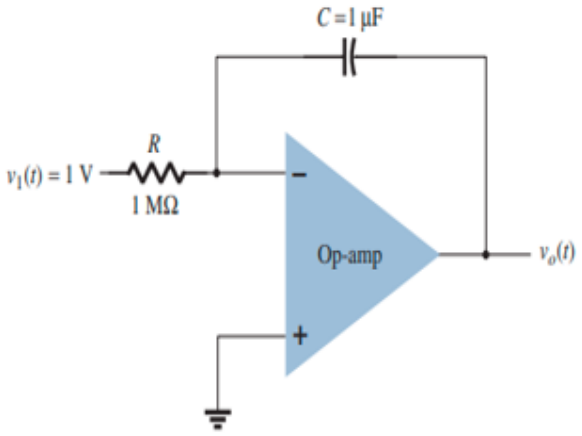
Q7. Determine the output voltage for the circuit of figure below with a sinusoidal input of 2.5 mV.

	1 V	A
	-025 V	B
	-0.75 V	C
	2 V	D

Q8. The operational amplifier circuit shown in the figure works as……..

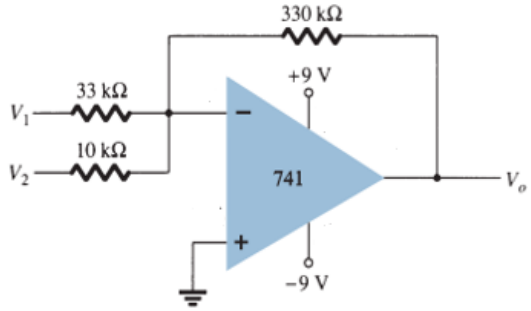
	Inverting amplifier	A
	Integrator	B
	Noninverting Amplifier	C
	Differentiator	D

Q9 . consider an input voltage V1 = 1 V to the integrator circuit of figure shown. The scale factor is…….

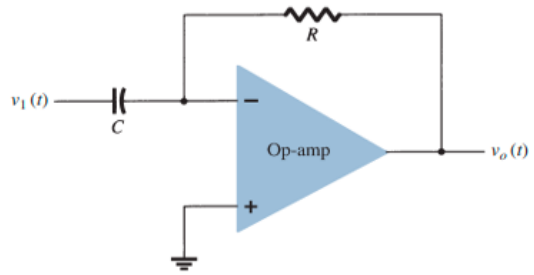
	-2	A
	1	B
	2	C
	-1	D

Q10. Calculate the output voltage for the circuit of figure shown. The inputs are V1= 50 mV sin(1000t) and V2= 10 mV sin(3000t)

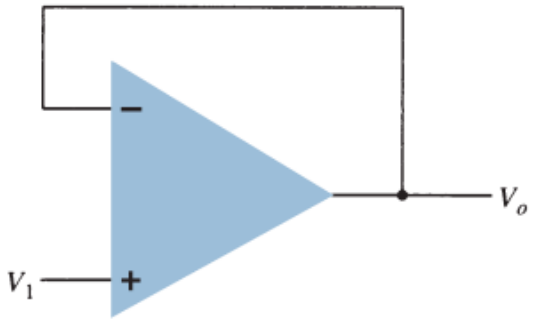
	Vo= 0.5 sin (1000t)+ 0.33 sin (3000t)	A

	Vo= -[5 sin (1000t)+ 33 sin (3000t)]	B
	Vo =5 sin (1000t)+ 33 sin (3000t)	C
	Vo= -[0.5 sin (1000t)+ 0.33 sin (3000t)]	D

Q11. The operational amplifier circuit shown in the figure works as……..

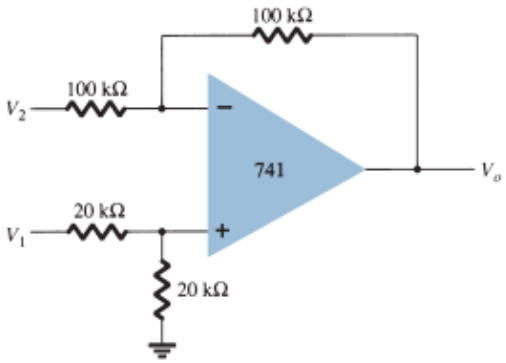
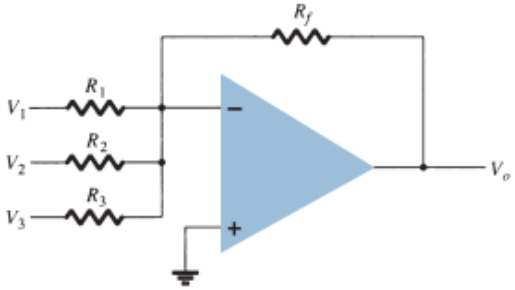
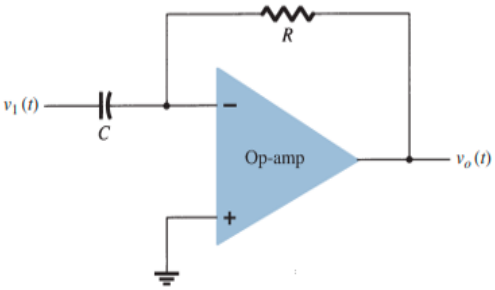
	Inverting amplifier	A
	Integrator	B
	Noninverting Amplifier	C
	Differentiator	D

Q12. For the Voltage Buffer shown , the output voltage is ……..

	Vo = -Vi	A
	Vo =Vi	B
	Vo = Zero	C
	Vo = ∞	D

Q13 Determine the output voltage for the circuit shown,if ,V1=20 mv and V2= 6 mv

	14 mV	A
	26 mV	B

	10 mV	C
	40mV	D
Q14 The ouput voltage of the circuit shown is……		
	Vo = - ($\frac{Rf}{R1}$V1 + $\frac{Rf}{R1}$V2 + $\frac{Rf}{R1}$V3)	A
	Vo = ($\frac{Rf}{R1}$V1 + $\frac{Rf}{R2}$V2 + $\frac{Rf}{R3}$V3)	B
	Vo = - ($\frac{Rf}{R1}$V1 + $\frac{Rf}{R2}$V2 + $\frac{Rf}{R3}$V3)	C
	Vo = ($\frac{Rf}{R1}$V1 + $\frac{Rf}{R1}$V2 + $\frac{Rf}{R1}$V3)	D
Q15. The scale factor of the circuit shown is…….		
	RC	A
	$\frac{-R}{C}$	B
	-RC	C
	$\frac{-1}{RC}$	D
Q19. When step- input is given to an OP-amp integrator, the output will be:		
	ramp	A

Sinusoidal wave	B
Rectangular wave	C
Triangular wave	D
Q20. In differential-mode,……	
the gain is one	A
the outputs are of different amplitudes	B
opposite polarity signals are applied to the inputs	C
only one supply voltage is used	D
Q21. In the differential voltage gain & the common mode voltage gain of a differential amplifier are **48db** & **2db** respectively, then its common mode rejection ratio is……..	
23dB	A
25dB	B
46dB	C
50dB	D
Q22. When a differential amplifier is operated single-ended,…….	
the output is grounded	A
one input is grounded and signal is applied to the other	B
both inputs are connected together	C
the output is not inverted	D
Q23. Negative feedback……..	
increases the input and output impedances	A

increases the input impedance and bandwidth	B
decreases the output impedance and bandwidth	C
does not affect impedance or bandwidth	D
Q24. A voltage follower ……	
has a voltage gain of 1	A
is noninverting	B
has no feedback resistor	C
has all of these	D
Q25. The closed-loop voltage gain of an inverting amplifier equal to……..	
the ratio of the input resistance to feedback resistance	A
the open-loop voltage gain	B
the feedback resistance divided by the input resistance	C
the input resistance	D
Q26. If ground is applied to the (+) terminal of an inverting OP-amp, the (-) terminal will ….	
Not need an input resistor	A
Be virtual ground	B
Have high reverse current	C
Not invert the signal	D
Q27. For Multiple-stage of operational amplifier circuits ,if we have 3-Stages the output gain is ……	
A=A1+ A2+ A3	A

A=A1 A2 A3	B
A=(A1 A2 A3) /3	C
A=A1+ A2+ A3/3	D
Q28. The ideal OP-amp has the following characteristics:	
Ri= ∞ ,Ro= 0 , A= ∞	A
Ri = 0 ,Ro = 0 , A = ∞	B
Ri = 0 ,Ro = ∞ , A = 0	C
Ri = ∞ ,Ro = ∞ , A = ∞	D
Q29. A noninverting closed loop op amp circuit generally has a gain factor ……	
less than one	A
greater than one	B
of zero	C
equal to one	D
Q30. The common mode voltage gain is ……..	
smaller than differential voltage gain	A
equal to differential voltage gain	B
greater than differential voltage gain	C
none of the above	D
Q31. A common mode signal is applied to …….	
the noninverting input	A

the inverting input	B
both inputs	C
top of the tail resistor	D
Q32. For an OP-amp having differential gain Av and common mode gain Ac the CMRR is given by:	
$A_d A_c$	A
$\frac{Ad}{Ac}$	B
$\frac{Ac}{Ad}$	C
$A_d + 1$	D
Q33. Which of the following amplifier is used in a digital to analog converter?	
Non inverter	A
Voltage follower	B
Summing Amplifier	C
integrator	D
Q34 The phase difference between the output and input signals in the inverting operational amplifier is equal to…. ……..	
270^0	A
0^0	B
90^0	C
180^0	D
Q35. The operational amplifier has an output impedance ……	
Less than 100Ω	A

Greater than 1 MΩ	B
Equal to ∞	C
Equal to 100 MΩ	D