وزارة التعليم العالي والبحث العلمي
الجامعة التقنية الوسطى
الكلية التقنية الهندسية الكهربائية

الامتحان المشترك 2024/2023
Subject: الكترونيك

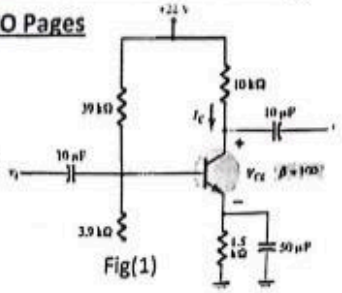
قسم هندسة تقنيات الحاسوب
التاريخ : 21 / 4 / 2024
وقت الامتحان : 90 دقيقة

Answer All Questions, the Questions are in TWO Pages

1) For the circuit shown in Fig (1):

R_{th} (in Fig 1) =

(A) 5.324 KΩ (B) 6 KΩ (C) 3.54 KΩ (D) 3.45 KΩ



Fig(1)

2) E_{th} (in Fig 1) =

(A) 2v (B) 3v (C) 1v (D) 4v

3) The condition for using the approximate technique in voltage divider bias is

(A) $\beta R_C \geq R_E$ (B) $\beta R_E \leq R_B$

(C) $\beta R_E \geq 10R_2$ (D) $\beta R_B \geq 10R_2$

4) I_B (in Fig 1) =

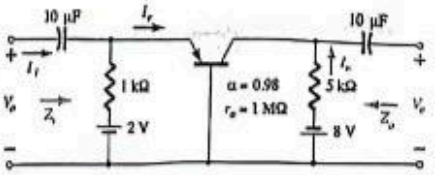
A) 5.38 μA (B) 1.83 μA (C) 8.38 μA (D) 4.29 μA

5. The phase difference between the output and input voltages of a CE amplifier is

(A) 180° (B)°0 (C)°90 (D) °270

6. For the fixed bias BJT configuration If Vcc=12 v, I_C= 2.35 mA and R_C=2.2kΩ, V_{CE}=

(A) 17.17 v (B) 4.2 v (C)-5.3 v (D) 6.83 v



Fig(2)

7) For the network of Fig(2) below, if I_E=1.3 mA, re= :

(A) 2 Ω (B) 8 Ω (C) 15 Ω (D) 20 Ω

8) The input impedance Z_i (in Fig 2) =

A) 20 Ω (B) 19.61 Ω (C) 1.8 Ω (D) 40.2 Ω

9) The voltage gain Av (in Fig2) =

(A) 150 (B) 100 (C) 250 (D) 80

10) The current gain A_I (in Fig2) =

(A) -0.98 (B) -0.99 (C) -1 (D) -100

11) Which resistor in a voltage divider configuration with a BJT transistor determines the output voltage?

(A) Base resistor (B) Collector resistor (C) Emitter resistor (D) Load resistor

12) For the fixed-bias JFET if I_D=10mA, V_{DD}=20 v R_D = 1.5 KΩ what is the value of the V_{DS}?

(A) 7.5 V (B) 4 V (C) 5.75 V (D) 5 V

13) The Shockley equation is

A) $I_D = I_{DSS}[1 - \frac{V_{GS}}{Vp}]^2$ (B) $I_D = I_{DSS}[1 - \frac{V_{GG}}{Vp}]^2$

(C) $I_D = I_{DSS}[2 - \frac{V_{GS}}{Vp}]^2$ (D) $I_D = I_{DSS}[1 - \frac{V_{GS}}{Vp}]^3$

وزارة التعليم العالي والبحث العلمي
الجامعة التقنية الوسطى
الكلية التقنية الهندسية الكهربائية

الامتحان المشترك 2024/2023
Subject: الكترونيك

قسم هندسة تقنيات الحاسوب
التاريخ : 21 / 4 / 2024
وقت الامتحان : 90 دقيقة

14) For a voltage divider bias A_v=

(A). $\frac{Rc}{re}$ (B) $\frac{Rc}{re+RE}$ (C) $\frac{RB}{RB+Zb}$ (D) $\frac{\beta RB}{RB+Zb}$

15) The Field Effect Transistor is called in this name because:

(A) Drain Current is controlled due to electric field Vgs (C) It is a unipolar device

(B) FET is smaller in size than BJT (D) FET has very high input impedance

16) The ac equivalent of a transistor network is obtained by Replacing all capacitors by-----

(A) Open circuit (B) short-circuit (C) Bypass capacitor (D) none of the above

17) Which of BJT transistor currents is the largest?

(A) I_C (B) I_E (C) I_B (D) I_D

18) Which of FET transistor currents should always be = 0?

(A) I_D (B) I_S (C) I_G (D) I_B

19) A JFET data sheet specifies VP = –10 V and IDSS = 8 mA. Find the value of ID when VGS = –3 V.

(A) 2 mA (B) 1.4 mA (C) 4.8 mA (D) 3.92 mA

20) For all FETs .....

(A) $I_D = I_S$ (B) $I_D = 0$ mA (C) $I_D = I_G$ (D) $I_S = I_G$

21) In re model of C.B. configuration Z_o=

(A) ∞ (B) β (C) 0 (D) None of above

22) Given β= 120 and I_E= 3.2 mA for a common-emitter configuration with r_o=∞ Ω. Determine Zi.

(A) 975kΩ (B) 0kΩ (C) 5kΩ (D) 1.2 kΩ

23) For an n-channel FET, What is the direction of current flow

(A)Source to drain (B)Drain to source

(C)Gate to source (D) Gate to drain

24) For the fixed-bias JFET with I_{DSS}= 10 mA, V_P= -8 v and V_{GG} = 2v , what is the value of the drain current ID?

(A) 6.250 mA (B) 2.650 mA (C) 5.625 mA (D) 100

25) For the FET transfer characteristics when $I_D = I_{DSS}$, then V_{GS} is

(A) -1.8 V (B) -3V (C) 0 V (D) -6V